ATMD-GPX

TDC-GPX Evaluation System

Datasheet

18TH MAY 2005

acam - solutions in time

Precision Time Interval Measurement

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Index

Limited Warranty

The ATMD measurement system with it's components ATMD-MB, ATMD-PC, ATMD-PCI and AM-GPX is designed and offered as an evaluation system for the integrated circuit TDC-GPX, offered by acam-messelectronic. The hardware are warranted against defects in materials and workmanship for a period of 12 months from the date of shipment, as evidenced by receipts or other documentation. acam-messelectronic will, at its option, repair or replace equipment that proves to be defective during the warranty period.

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CE

The products ATMD with its components comply with EMC directive 89/336/EEC, applied standard DIN EN 61326, Equipment for Control and Laboratory (For use in electromagnetically controlled environment). Generic immunity standard part 2 (EN 61000-4-4: 0,5KV, -4-6: 1V), In case of strong electromagnetic disturbances there might be a deviation of the ouput signal from the specification, but only for the duration of the disturbance.

1. Introduction

1.1 System overview

The ATMD-GPX evaluation system consists of a motherboard together with the AM-GPX plug-in module, mounted in a metal case. It is connected to the ATMD-PCI interface card (mounted in the PC) by a SCSI-type cable (although the bus is ATMD specific and not a PCI type).

Ordering numbers:

ATMD-GPX	MNR 881	Motherboard with 1 AM-GPX plug-in module incl. Software, manuals and cables
ATMD-PCI	MNR 478	PCI interface

Features ATMD

- Two operating modes
  - Direct Read
  - Burst Mode
- FIFO on motherboard 1K (can be increased to 32K)
- Supply through PCI interface
- Op. temperature range –25°C ... +70°C
- Maximum data rate PCI interface about 1 MHz, depending on software.

Features AM-GPX

Three operating modes

- I-Mode
  - 8 channels with 81 ps resolution
  - 5.6 ns pulse-pair resolution with 32-fold multihit capability
  - LVTTL inputs
- G-Mode
  - 2 channels with 40 ps resolution
  - Measuring falling and rising edge, minimum pulsewidth 1.8ns
  - 5.6 ns pulse-pair resolution with 32-fold multihit capability
  - Differential LVPECL inputs, LVTTL inputs for testing
  - Optional quiete mode
- R-Mode
  - 2 channels with 27 ps resolution
  - Measuring falling or rising edge
  - 5.6 ns pulse-pair resolution with 32-fold multihit capability
  - Differential LVPECL inputs, LVTTL inputs for testing
  - Optional quiete mode
- M-Mode
  - 2 channels with 10 ps resolution
  - Measuring falling or rising edge
  - single stop pulse
  - Differential LVPECL inputs, LVTTL inputs for testing
  - Quiete mode

1.2 Hard- and Software Installation

Important! All components of the ATMD-System are sensitive to static electricity. Before installing the interface board, please touch a grounded object such as a metal screw on the computer. Handle the interface board by its edges and be careful not to twist it.

Perform the following steps to install the interface board:

1. 🗁 ni-visa
   ----------Nivisa.msi — run NI Visa instrument drivers installer

2. lvruntimeeng.msi — run NI LabView runtime installer for Windows 98
   or
   visa320runtime.exe — run NI LabView runtime installer for Windows NT/2000/XP

3. Turn off your computer. Keep your computer plugged in so that it remains grounded while you install your interface board. Remove the computers cover. Next , align the interfaces edge connector with an 32-bit PCI expansion slot for ATMD-PCI. Then, push the board down into the slot until the board locks into place. It might be a tight fit, but do not force the board into place. Screw the mounting bracket of the interface board to the back panel rail of the computer, check the installation and replace the cover of the computer.

4. Connect the interface board and the external ATMD motherboard via the enclosed cable (for convenience a standard SCSI-2 cable is used, but it is not a SCSI interface!) and turn on your computer.

5. The operating system will ask for a driver. Select from
🗁 AcamAtmdPCI — Inf-Files for registration of PCI-interface under NT/2000/XP
   ----------ATMD_PCI_9X.inf — for Windows '98
   ---------- ATMD_PCI_NT5.inf — for Windows NT, 2000, XP

6. 🗁 ATMD_GPX_4_0
   ----------🗁 Installer
   ----------setup.exe — run installer for ATMD-GPX software

7. To start the ATMD-GPX software select START/Programs/ATMD_GPX_4_0/ ATMD_GPX_4_0.

If you want to write your own C++ based software install the following files for a free access to the I/O ports:

🗁 Driver
   ----------instdrv.exe — copies giveio.sys and windrvr.sys into the System32\drivers folder
   When working with Windows NT/2000/XP first install the necessary drivers executing instdrv.cmd. Open the device manager, select menu item 'Show hidden devices' and select folder 'Non-PNP devices'. There you will find the giveio.sys and windrvr.sys. Select under properties the start option 'automatic'.
🗁 PCI
   ----------atmd_pci.dll — copy this file into system folder
   ----------atmd_pci.lib — "

Furhter files on the CD-ROM are:

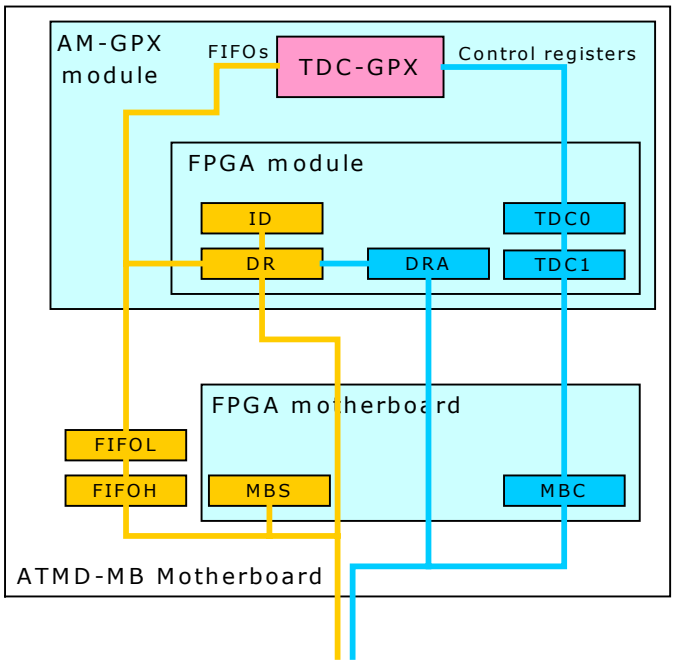
🗁 Samples
   ----------G-Direct-TTL etc. — Visual C++ samples
🗁 Doc — all available documents in PDF-format

2. Writing Software

2.1 ATMD Registers

For the communication between PC and TDC-GPX there are several registers on the motherboard FPGA and the AM-GPX module's FPGA.

To setup the TDC-GPX control registers write into registers TDC0 and TDC1. There are two possible ways to read out data from the TDC-GPX: a) Direct read by registers DRA and DR. The TDC must be reinitialized after by sending a partial or master reset. b) Burst mode: the module FPGA controls the measurement. It makes the TDC write the data into the motherboard FIFO and reinitializes the TDC automatically. The user reads the data from the motherboard FIFOs.



2.1.1 Register Addresses

Address Offset	Read		Write	
0x0	**DR**	Direct Read	**TDC0**	GPX data
0x2		n.a.	**TDC1**	GPX data + Adr
0x4	**ID**	Module Identification	**DRA**	Direct Read Address
0x6		n.a.		n.a.
0x8	**MBS**	Motherboard Status		n.a.
0xA	**FIFOL**	FIFO LSW		n.a.
0xC	**FIFOH**	FIFO MSW	**MBC**	Motherboard Control

2.1.2 Register Structure

Write Registers

Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDC1	A3	A2	A1	A0	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
DRA	-	-	-	-	-	-	-	-	-	-	-	-	A3	A2	A1	A0
MBC	-	-	-	-	-	-	BMH	RS	-	-	-	Trig	Dis	St01	BML	RS

Read Registers

Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MBS	1	1	1	TEF2	TEF1	BMH	FFH	EFH	-	-	TINT	-	-	BML	FFL	EFL
ID	C2	C1	C0	0	0	0	0	0	0	0	0	0	0	0	0	0
FIFOL	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FIFOH	St01	IF#	-	-	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

2.1.3 Registers in Detail

All register bits are active high except the FIFO flags FFH, EFH,FFL and EFL!

TDC0	D0 to D15	Data to be written into TDC-GPX control registers, bits D0 to 15
TDC0	D16 to D27	Data to be written into TDC-GPX control registers, bits D16 to 27
	A0 to A3	Address of TDC-GPX control register
DRA	A0 to A0	Address of TDC-GPX read register
MBC		Motherboard Control register (write)
	BMH,L	0x0202 = Burst Mode on
	RS	0x0101 = Module Reset
	St01	1 = output of actual Start01 value, indicated by highest Bit of FIFOH = "0"
	Dis	1 = hardware disable of all inputs (sets StartDIs and StopDisx pins of TDC-GPX
	Trig	1 = crate pulse at pin 4 of connector 11, can be used to trigger external pulse generator
MBS		Motherboard Status register (read)
	EFH,L	Motherboard FIFO Empty (High Word, Low Word) low active
	FFH,L	Motherboard FIFO Full (High Word, Low Word) low active
	BMH,L	Burst Mode (High Word, Low Word)
	TEF1,2	Empty flags of TDC-GPX interface FIFOs
	Tint	TDC-GPX interrupt flag
ID		
	C[2:0]	Module code, AM-GPX = '100' (ID = 0x8000), to be used for automatic module detection.

FIFOL, FIFOH

Output Data Format

D0 to D27	represent the TDC-GPX output data. The format depends on the measurement mode. For details see the TDC-GPX manual.
IF#	indicates from which TDC-GPX interface FIFO the are. "0" = IFIFO0, "1" = IFIFO1
St01	"1" = time measurement data, "0" = Start01 value (I-Mode)

If one of the FIFOs rises it's full flag, the AM-GPX Module stops writing to them. Therefore FIFOL and FIFOH must always be read together to avoid an unbalanced number of values in the FIFOs.

If FIFOL and FIFOH are not read together it can lead to:

Uncorrelated data:	channel number and time value do not belong to each other!
Loss of data:	the full FIFO disables also writing data to the other FIFO

2.2 Direct Read Mode

In this mode the software communicates directly with the TDC-GPX. The user reads the output data directly from the TDC-GPX interface FIFO's.

The following example for G-Mode shows how to wirte software for the ATMD-GPX:

1. Get base address of the ATMD-PCI interface card

```
#include "atmd_pci.h"

// detect ATMD PCI (call GetATMDPCIBoardCount()
// to detect number of ATMD-PCI boards)

iBoardCount = GetATMDPCIBoardCount();
printf("No. of ATMD PCI boards found = %d\n",iBoardCount);

i=0;
while((!AtmdOK) || (i>4))
{
      AtmdOK = GetATMDPCIBaseAddr(i,dwTemp);
      atmd_pci_base_address[i] = (WORD) dwTemp;
      i++;
}
if (AtmdOK)
{
      printf("ATMD PCI Board found on 0x%x\n",atmd_pci_base_address[i-1]);
      base = atmd_pci_base_address[i-1];        // base = base address
      if(!EnablePortAccess())
      {
            AfxMessageBox("Giveio.sys couldn't be opened");
      }
}
else
{
      AfxMessageBox("ATMD-PCI interface not found");
}
```

2. Board reset

```
//  ******************** board-reset ******************
_outpw(base+0xC,0x0101);
Sleep(1);
_outpw(base+0xC,0x0008);
```

Write into the Motherboard control register, setting bits "RS" (D0 and D8) to [1] and back to [0].
Set the "Dis" bit in the motherboard control register. This one disbles all inputs of the TDC-GPX by hardware.

3. Set the TDC-GPX control registers

The ATMD registers are 16 bit wide. As the TDC-GPX write registers are 28 bit wide, we have to write twice. The first write command is into ATMD write register TDC0. We write bits 0 to 15 of the register content. The second write command is into ATMD register TDC1. We write the bits 16 to 27 of the register content and as highest four bits the address. With the second write command the FPGA on the AM-GPX module combines the data and transfers the full register content to the address of the TDC-GPX.

```
// ****************** Setup ***************************
//                     _LSB                   ___Address
//                    |                     | _____MSB
//                 ...|                     ||..
_outpw(base+0x0, 0x10FB);_outpw(base+0x2, 0x0000);
      //Reg 0, Start ring oscillator, enable & falling rising edges
_outpw(base+0x0, 0x0700);_outpw(base+0x2, 0x1707);
      //Reg 1, Set the channel adjust bits bits for best standard deviation
_outpw(base+0x0, 0x0001);_outpw(base+0x2, 0x2007);
      //Reg 2, select G-Mode, set channel adjust bits
_outpw(base+0x0, 0x0000);_outpw(base+0x2, 0x3800);
      //Reg 3, use TTL inputs (G-Test)
_outpw(base+0x0, 0x0100);_outpw(base+0x2, 0x4600);
      //Reg 4, Mtimer begins with Start, empty flags driving all the time, quiet
      mode
_outpw(base+0x0, 0x0000);_outpw(base+0x2, 0x5000);
      //Reg 5, Start Offset 1
_outpw(base+0x0, 0x8000);_outpw(base+0x2, 0x6800);
      //Reg 6, Switch on ECL inputs
_outpw(base+0x0, 0x1FCE);_outpw(base+0x2, 0x7014);
      //Reg 7, Resolution = 35.9583 ps (71.9166/2 in G-Mode)
_outpw(base+0x0, 0x0000);_outpw(base+0x2, 0xB400);
      //Reg 11,PLL not locked -> Err
_outpw(base+0x0, 0x0000);_outpw(base+0x2, 0xC200);
      //Reg 12,MTimer -> Int
Sleep(500); // Give PLL time to lock
```

The TDC-GPX is set to G-Mode. We use the TTL inputs.
The Mtimer is started by the START input. It is set to 40 x 25ns = 1 µs. At the end of the Mtimer the interrupt flag is set.
If the PLL is not locked the error flag is set.

4. Measurement

```
_outpw(base+0x0,0x0000);_outpw(base+0x2,0x4640);//TDC-GPX MasterReset
printf("TDC resetted");

do
{
      while(!(_inpw(base+0x8) & 0x0020)); // Check Interrupt flag
      _outpw(base+0xC,0x0018);  // disable inputs and trigger the ALU trigger
      _outpw(base+0x4,0x000B);  //Read register 11, get number of hits per channel
      N0 = _inpw(base+0x0);
      N1 = ((N0 & 0xFF00)>>8)*2;  // # of Hits in register 8
                                  // *2 as rising and falling edge is selected
```

```
      N0 = (N0 & 0xFF)*2;      // # of hits in register 9
                               // *2 as rising and falling edge is selected
      printf("N0 %X\tN1 %X\n",N0,N1);

      i=0;
      while(i<N0)  //read data directly from TDC-GPX read register 8
      {
            _outpw(base+0x4,0x0008); //Read TDC-GPX IFIFO1
            FIFO0 = _inpd(base+0x0)&0x7FFFFF;
            Edge = (FIFO0 & 0x400000)>>22;
            FIFO0 = FIFO0 & 0x3FFFFF;
printf("ch1 hit# %d Edge %d  \t%5.3fps\n",i+1, Edge,(FIFO0-150)*35.958/1000);
            i++;
      }

      i=0;
      while(i<N1)  //read data directly from TDC-GPX read register 9
      {
            _outpw(base+0x4,0x0009); //Read TDC-GPX IFIFO2
            FIFO1 = _inpd(base+0x0)&0x7FFFFF;
            Edge = (FIFO1 & 0x400000)>>22;
            FIFO1 = FIFO1 & 0x3FFFFF;
printf("ch2 hit# %d Edge %d  \t%5.3fps\n",i+1, Edge,(FIFO1-260)*35.958/1000);
            i++;
      }

      _outpw(base+0xC,0x0000);  // enable inputs
      _outpw(base+0x0,0x0000);_outpw(base+0x2,0x4640);//TDC-GPX MasterReset
} while ( !quit );
```

This routine waits until the interrupt flag is set. In the following it checks the number N of hits (in G-Mode the falling edges are counted). Finally it reads N times directly from the TDC-GPX output registers.

2.3 Burst Mode

In this mode the software writes directly to the TDC-GPX but reads from the motherboard FIFOs. The measurement itself is controlled by the AM-GPX FPGA.

The difference to Direct Read Mode is only in the measuring routine:

```
//TDC-GPX MasterReset
_outpw(base+0x0,0x0000);_outpw(base+0x2,0x4640);

_outpw(base+0xC, 0x0202);     //Burst mode on

do
{
      while(!(_inpw(base+0x8) & 0x0101)); //check motherboard empty flags

      FIFO0 = _inpw(base+0xA);      // read from the first 16 bit FIFO block
      FIFO1 = _inpw(base+0xC);      // read from the second 16 bit FIFO block

      Chan = ((FIFO1 & 0x4000)>>14);
      TimeBins = ((FIFO1 & 0x7F)<<16) + FIFO0;
      Time = float(TimeBins) * 72.62 / 3 / 1000;

      printf("%d  %X %5.3f\n",Chan,TimeBins,Time);

} while ( !quit );

// ********************************* End of Your code
*****************************************
_outpw(base+0xC, 0x0000);     //Burst mode off
```

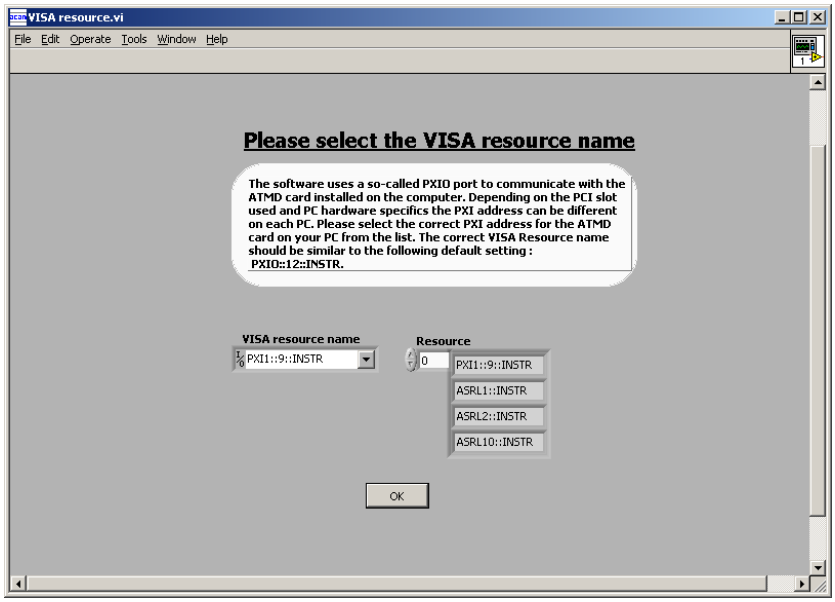
As soon as the Burst mode is switched on it is not possible to communicate directly with the TDC-GPX. Only the motherboard control register MBC is accessible. The data are available from the motherboard FIFO's.

The TDC-GPX read address (8 or 9 for the interface FIFOs) is coded in FIFO1, bit 14. [0] stands for TDC-GPX register 8, [1] for register 9.

3 ATMD_GPX Measurement Software

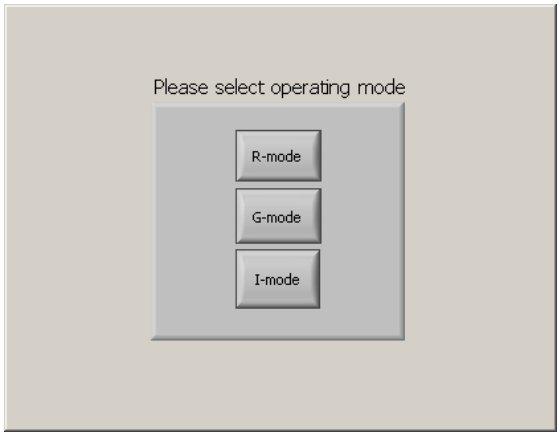
3.1 Measurement Software

1. When starting the ATMD software the user is first asked to select the right PCI interface card for communication:



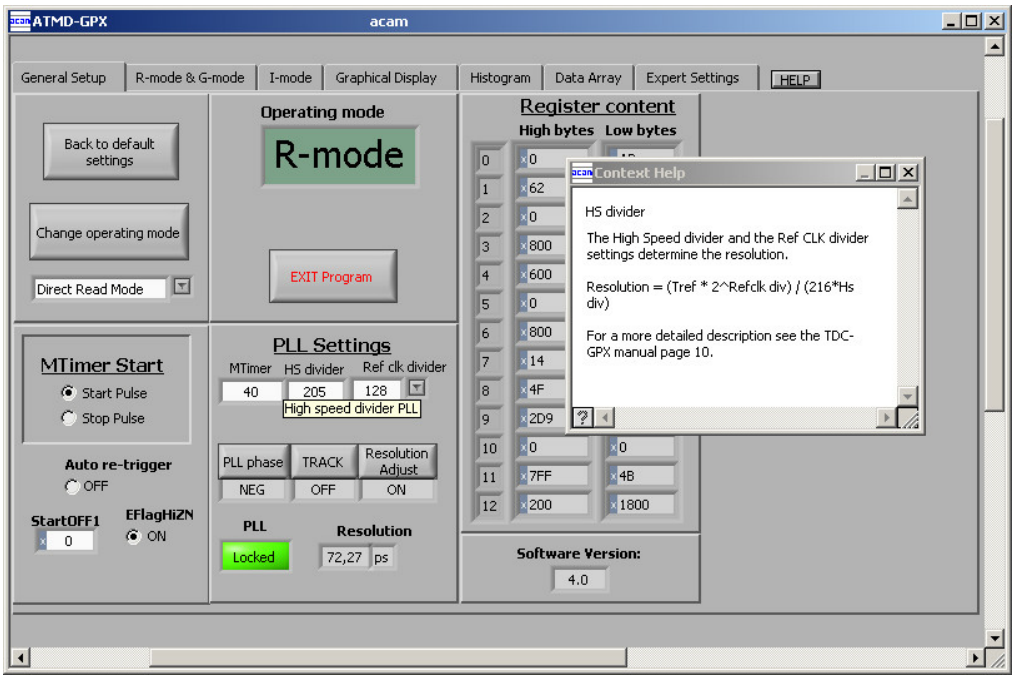
Please select a PXI... device and press ok. Now the main software page is shown.

2. Next you are asked to select the operating mode:



The mode can of course be changed later also. M-Mode is a subroutine of R-Mode.

3. The first page of the ATMD-GPX software shows general setup items.



When you move the mouse over a button, a short description of the button will be displayed. For further information the user can activate additional information by pressing the HELP button in the upper right corner. A small window with more information will be displayed.

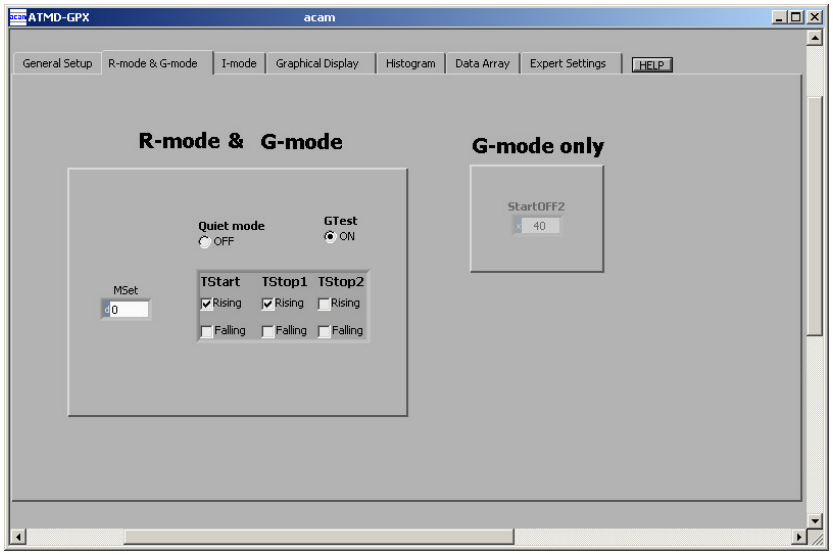
4. The first selection should be between "Burst Mode" and "Direct Read Mode". A change will set back all other items to the default settings.
"Direct Read Mode": The software communicates directly with the TDC-GPX.
"Burst Mode": An FPGA controls the measurement. The software looks for data in the motherboard FIFOs only. This speeds up the measurement rate drastically.

5. The second selection should be about "Auto re-trigger".
- on: the StartRetrig Bit of the TDC-GPX is set. The Start input can be retriggered. All timings refer to the last Start. This option works only in combination with StartTimer = 1 (see I-Mode page). With "Auto re-trigger" the external pulse generator need not be synchronized with the ATMD. It is recommended to use this option.

- off: The TDC-GPX should get only one start pulse. In the ATMD-GPX software the TDC-GPX interrupt is created by the "Mtimer". On this page the user selects the way the "Mtimer" is started as well as the time interval in multiples of 25ns. In this example "Mtimer" is triggered with a START pluse and runs for 40 * 25ns = 1µs. The values for HS Divider and Ref clk divider set the resolution which is displayed. PLL phase is “NEG” with the regulator circuit used on the board. This option asks for a synchronization between ATMD and external pulse generator. Therefore the AM-GPX module has a connector to send a trigger pulse to an external device (Jxx, control by MBC register Blt "Trig").

6. Setting the resolution: The resolution can be changed in a limited range, typically between 71 to 90 ps, depending on the TDC-GPX chip. The displayed resolution always refers to the I-Mode bin size. In R-Mode the Bin size is the displayed value divided by 3 (In the figure shown above the Bin size would be 72.27/3=24,09 ps. "Ref-Clk-divider" should be 128, "HS divider" should be in the range of 180 to 205.

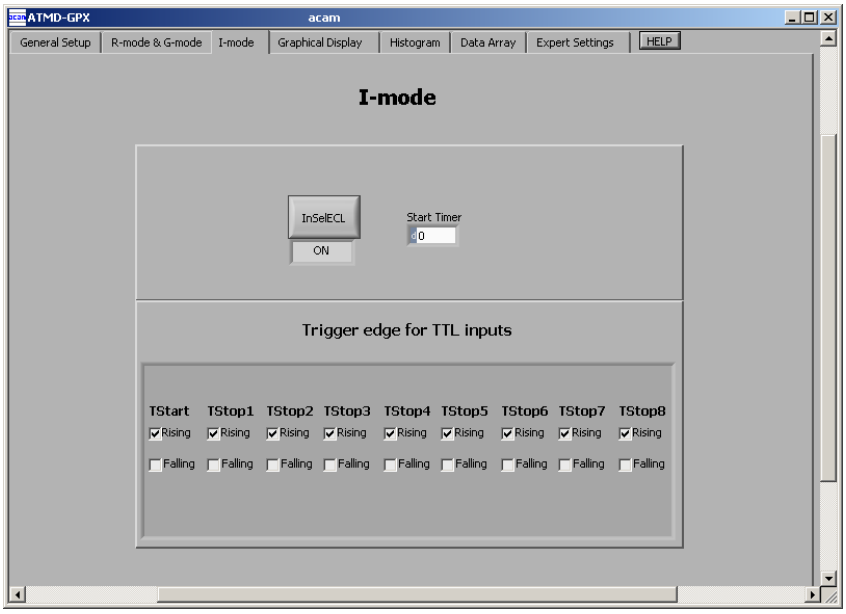
7. R- and G-Mode page



On this page the user sets the sensitivity of the inputs to a) rising or falling edge in R-Mode b) rising and/or falling edge in G-Mode.
With “Quiet mode selected” the ALU starts data processing not before the interrupt flag has come.
With “Gtest” selected the LVTTL inputs are used instead of the LVPECL inputs.

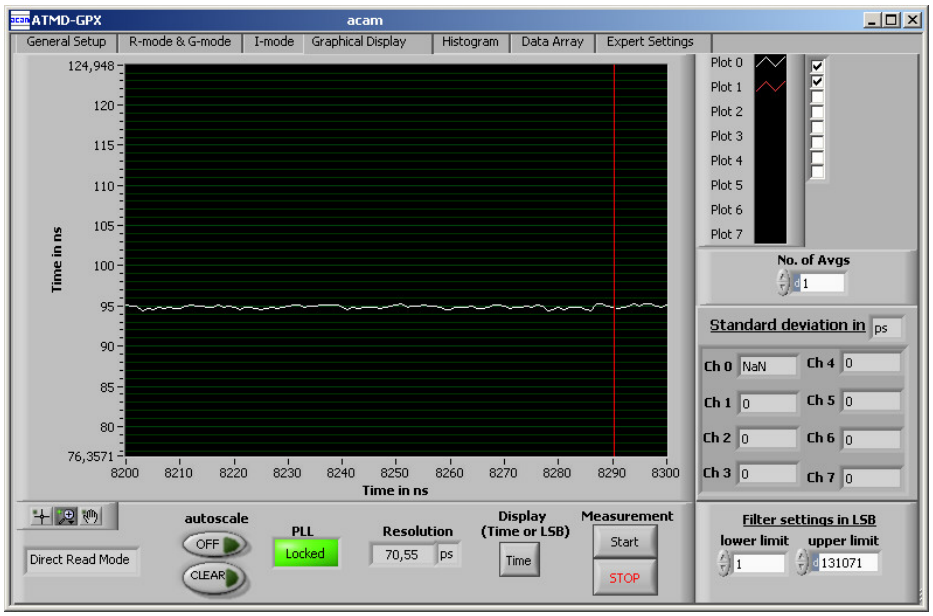
Setting MSet > 1 activates the M-Mode. This works only in combination with Quiet mode.

8. I-Mode page



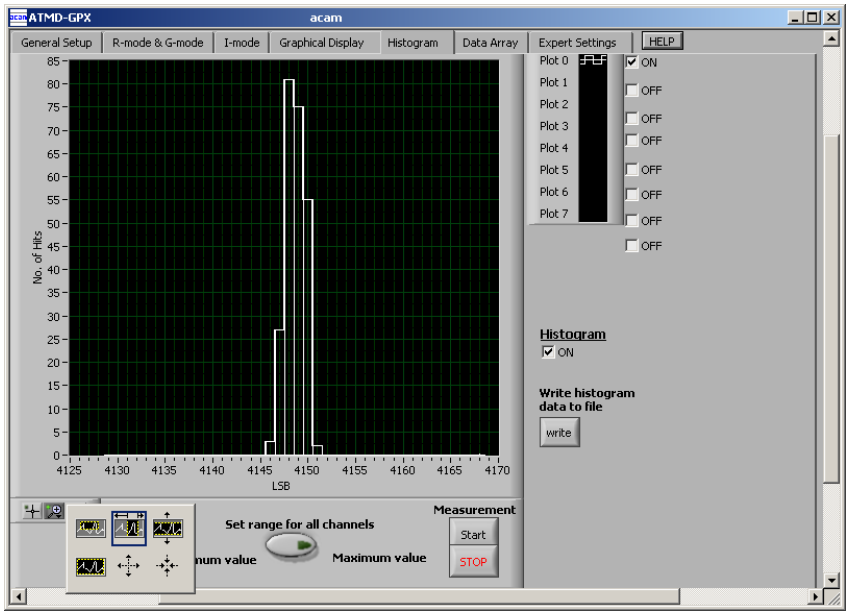
On this page the user sets the sensitivity of the inputs to rising or falling edge in I-Mode.
With “InSelECL” selected the LVPECL inputs are used instead of the LVTTL inputs.
DSTOP1 is switched to Tstop1, Tstop3, Tstop5, Tstop7, DSTOP2 is switched to Tstop2, Tstop4, Tstop6, Tstop8.
Start Timer defines the period between two internally generated start pulse. "0" switches off the internal start pulse generation. "1" is necessary for the external start retrigger. Higher values set the internal start retrigger.

9. Graphical Display page:



This page is for the graphical display, showing the measurement results (y) over runtime (x).
The scales can be modified directly by editing the corner values or by using the magnifying glass tool.
The filter is a software filter. It is useful in applications where the pulse generator is not synchronized with the software.
"No. of Avgs" activates software averaging. The standard deviation always refers to the single shot measurement.

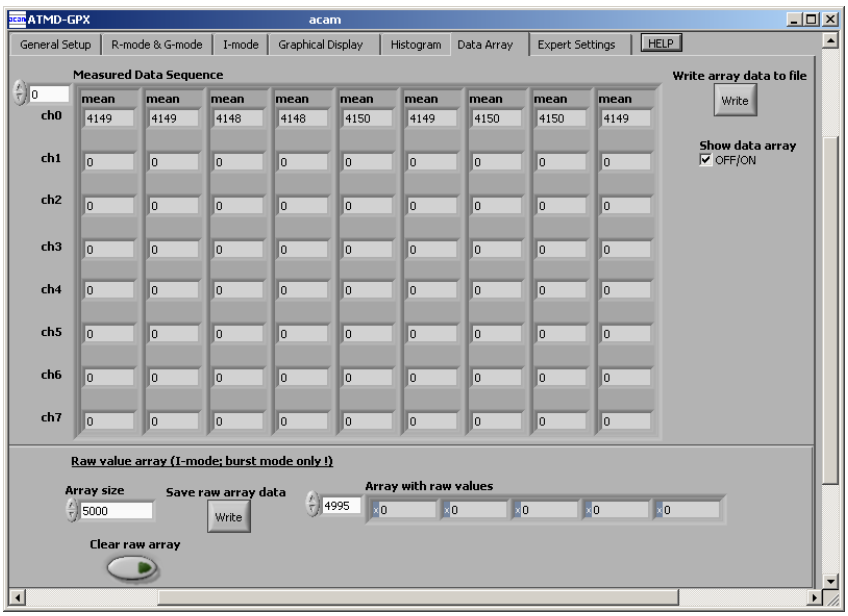
10. Histogram page



This page shows the measurement data as a histogram (hits per time slot). For speeding up the measurement the histogram is by default be switched off.

When starting the histogram press "Set range for all channels" button and then select "full display" item from the loop (lower left). For a full resolution histogram select LSB display on the graphical display page. Otherwise the resolution of the histogram display is limited to 1ns.
There is also a possibility to export the histogram data.

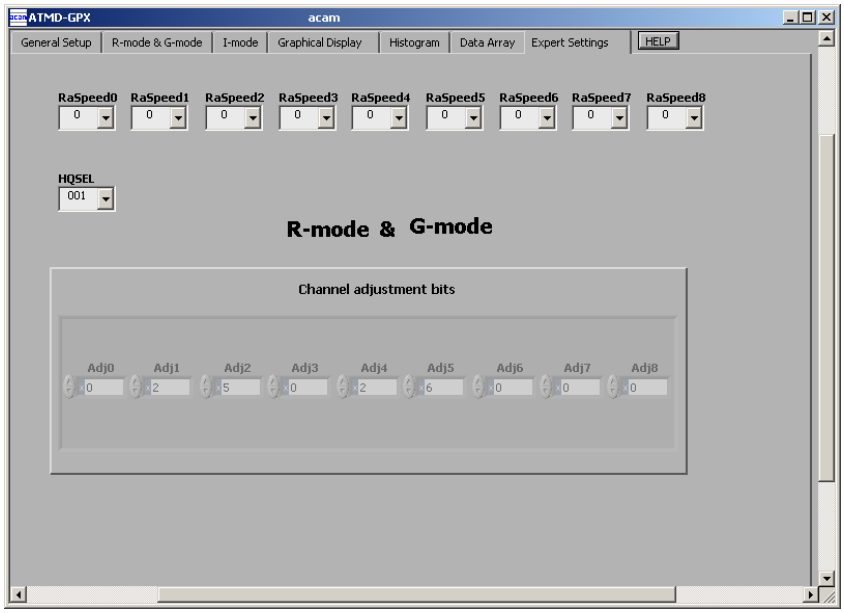
11. Data array page



The software collects the latest 1024 data that are displayed. They can be exported into a file. In case there are more than one active stop channels, only one channel has a new value, the other channels keep the latest value. This is necessary to have a comfortable display.

To overcome this data manipulation there is a possibility to write the pure TDC raw data into a file. The size of the raw data array can be selected.

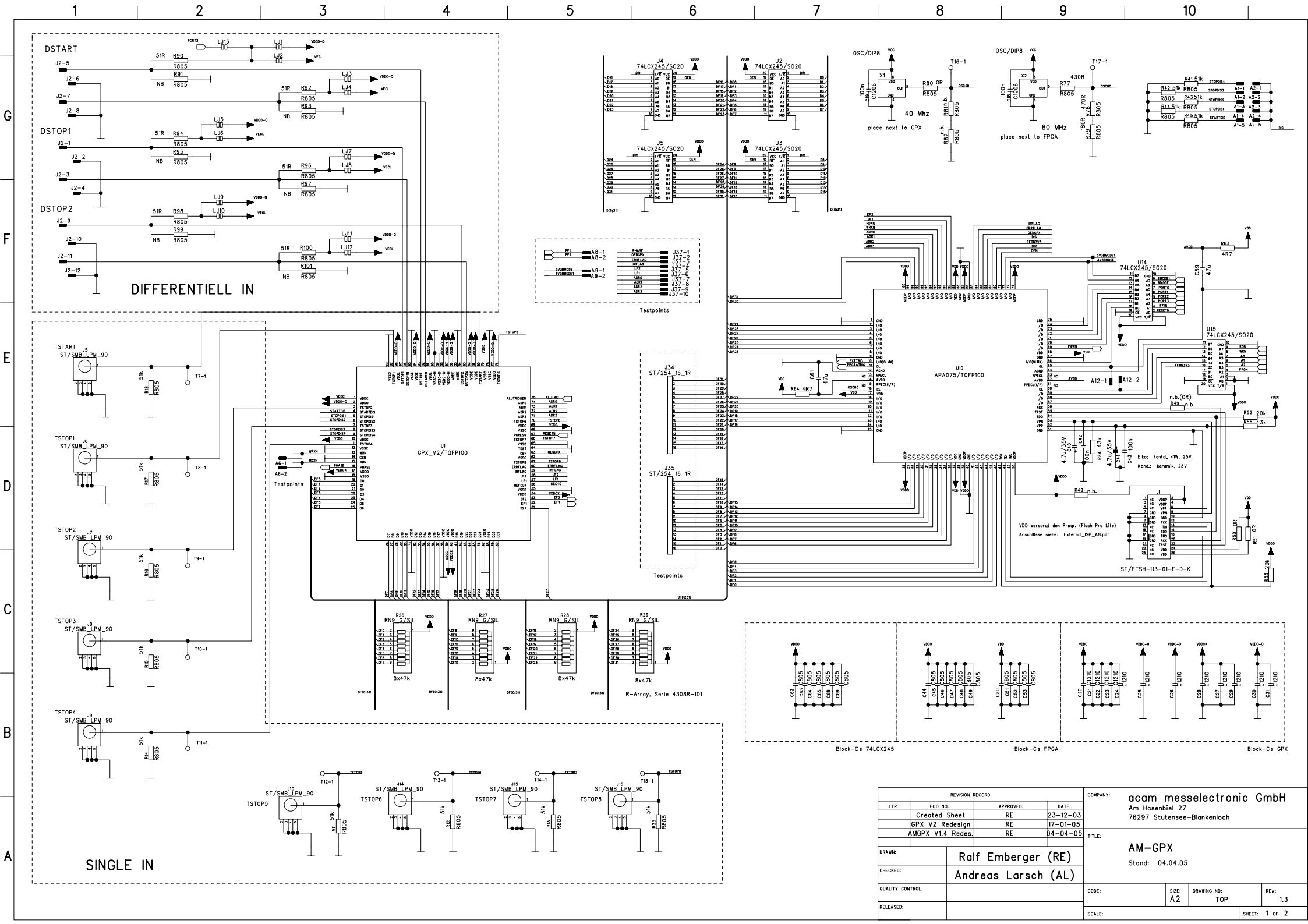
12. Expert settings page



This page is used in R- and G-Mode to set the adjustment bits for best standard deviation. We recommend to use the default values.

4 AM-GPX module

4.1 AM-GPX Schematics



REVISION RECORD			
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	Created Sheet	RE	23-12-03
	GPX V2 Redesign	RE	17-01-05
	AMGPX V1.4 Redes.	RE	04-04-05

DRAWN:	Ralf Emberger (RE)
CHECKED:	Andreas Larsch (AL)
QUALITY CONTROL:	
RELEASED:	

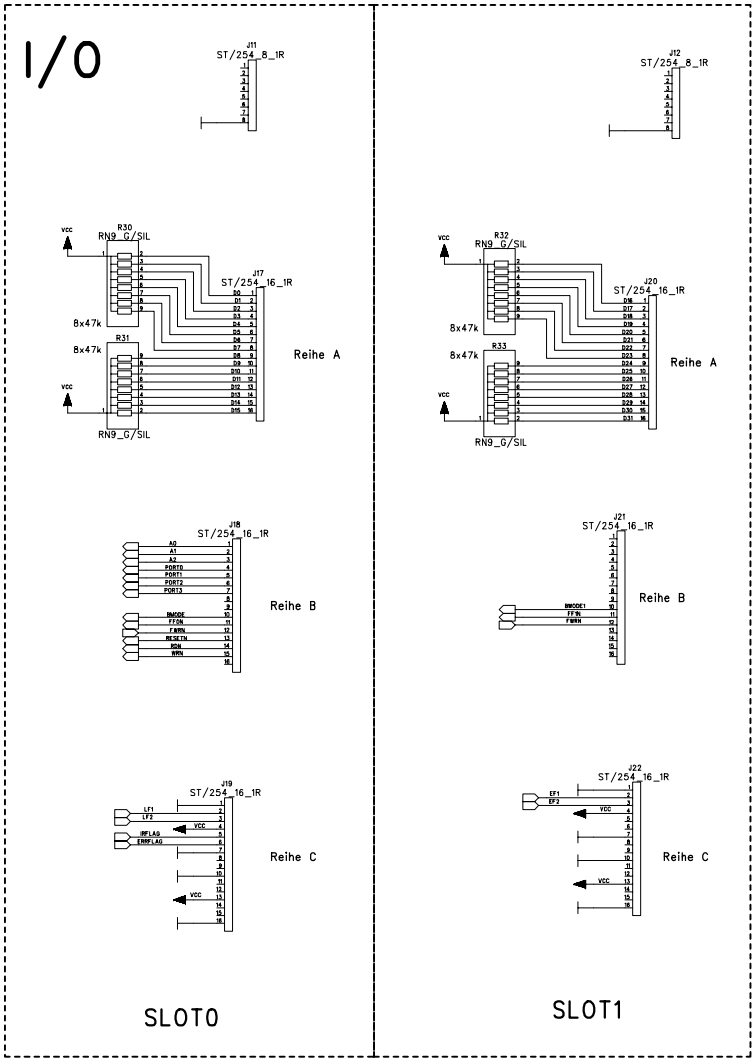
COMPANY: acam messelectronic GmbH
Am Hasenbiel 27
76297 Stutensee-Blankenloch

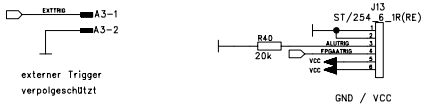
TITLE: AM-GPX
Stand: 04.04.05

CODE:	SIZE:	DRAWING NO:	REV:
	A2	TOP	1.3

SCALE: SHEET: 1 OF 2

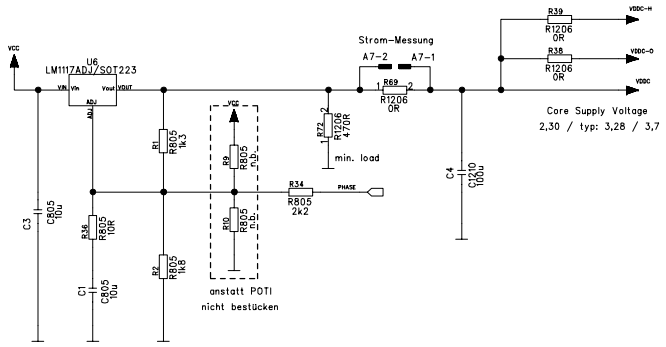
I/O



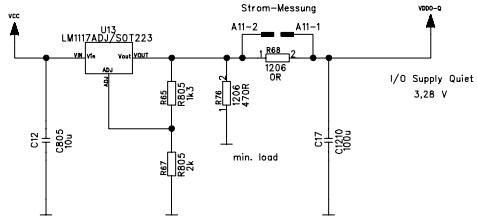


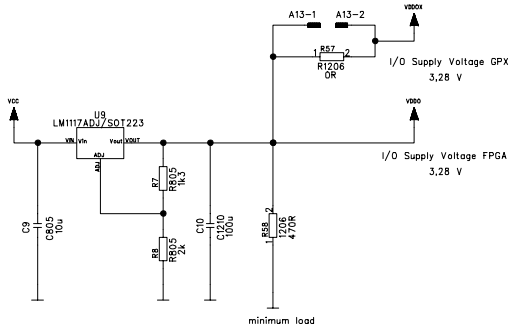
POWER SUPPLY

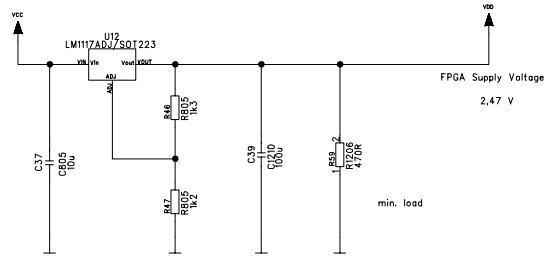
Note:
Vout = Vref x (1 + (R2/R1)) + Iadj. x R2
Vout = 3,3 V (typ): R1 > 100 Ohm; Iadj. = 55 uA (typ.)
siehe Datenblatt LM1117, Seite 9

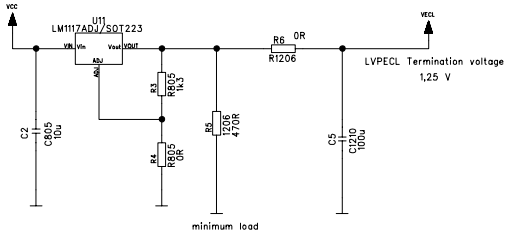


neue R1/R2/R34 Beschaltung
für erweiterten VDDC-Bereich









REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
	Created Sheet	RE	23-12-03
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DRAWN:	Ralf Emberger (RE)
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QUALITY CONTROL:	
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COMPANY: acam messelectronic GmbH
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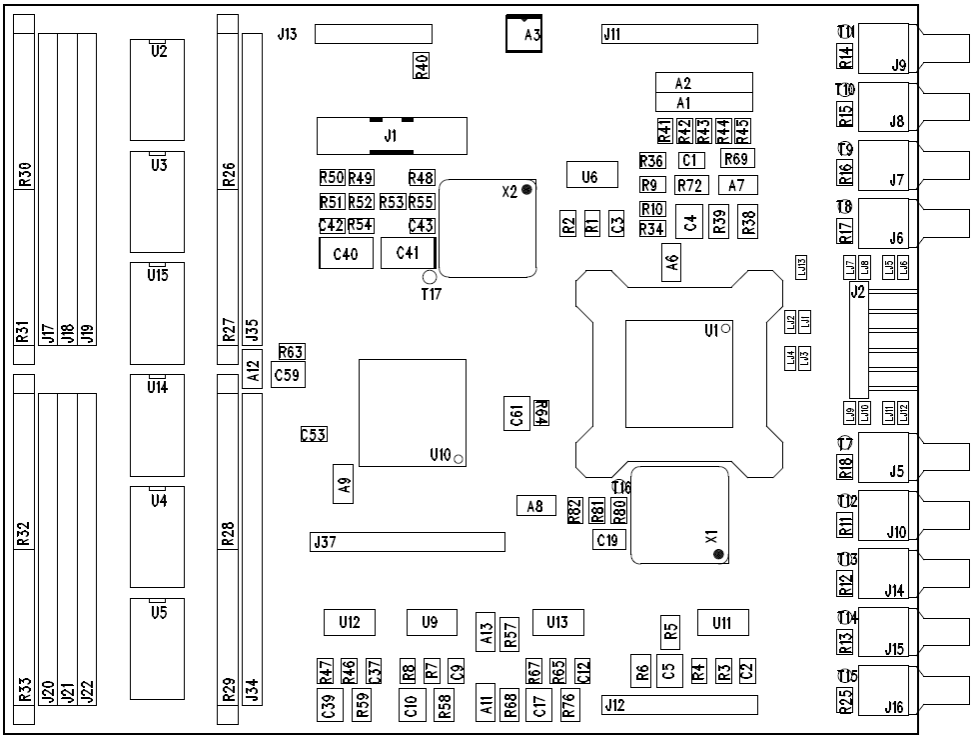
TITLE: AM-GPX
Stand: 04.04.05

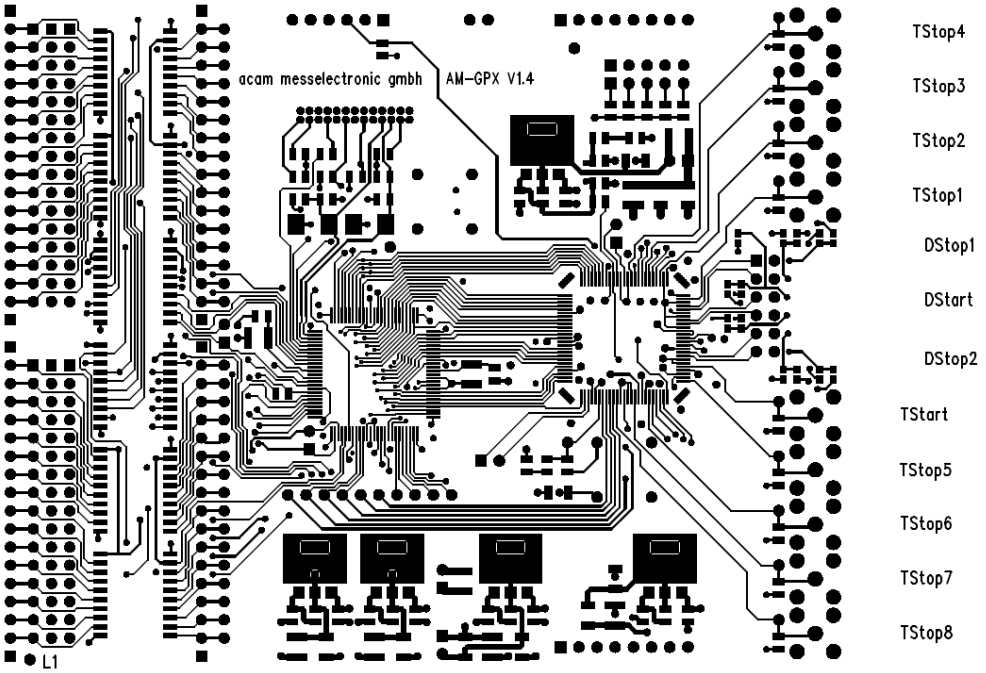
CODE:	SIZE:	DRAWING NO:	REV:
	A2	POWER_IO	1.2

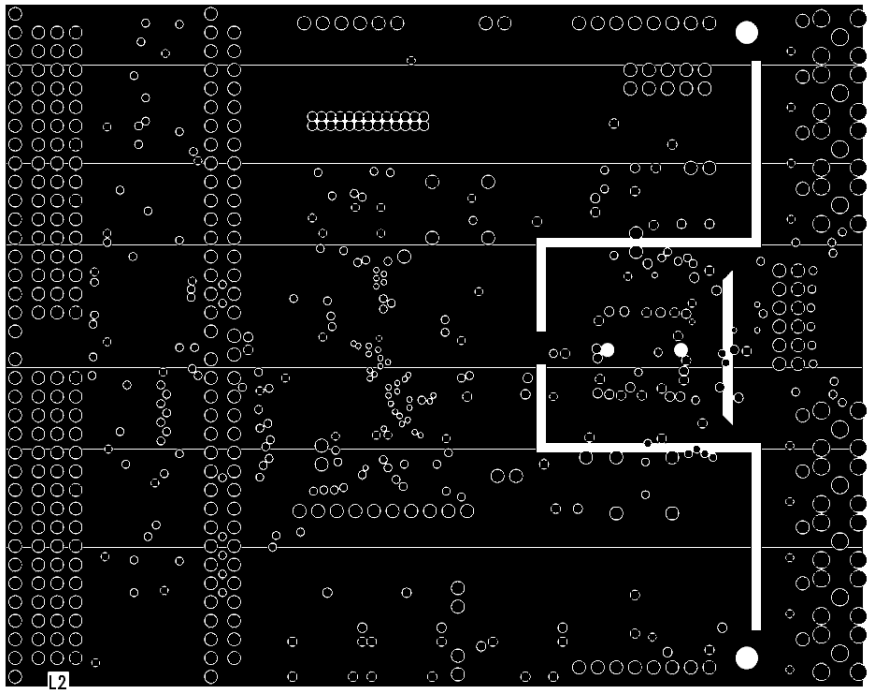
SCALE:

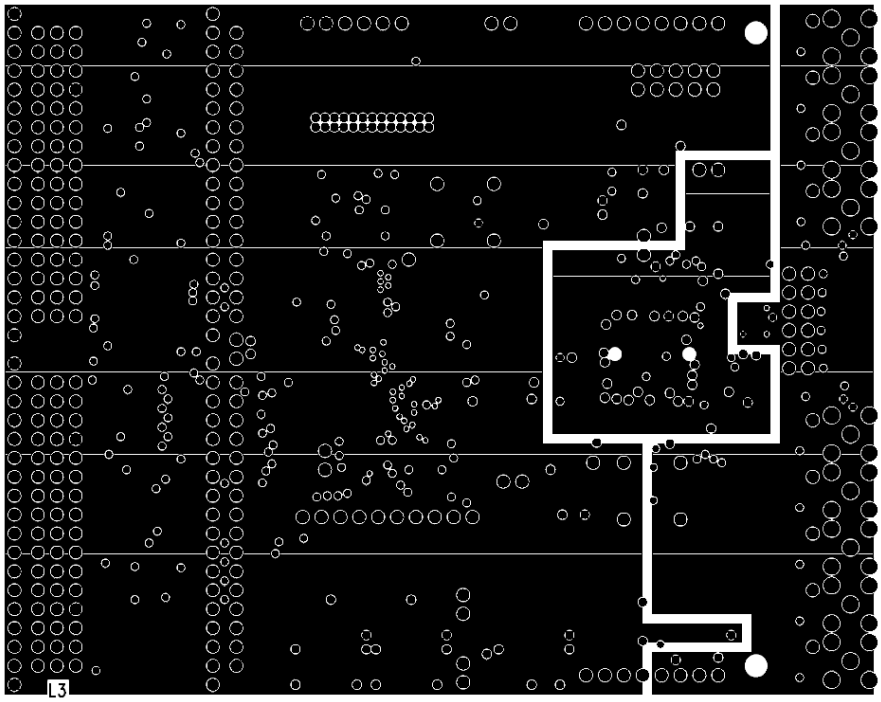
SHEET: 2 OF 2

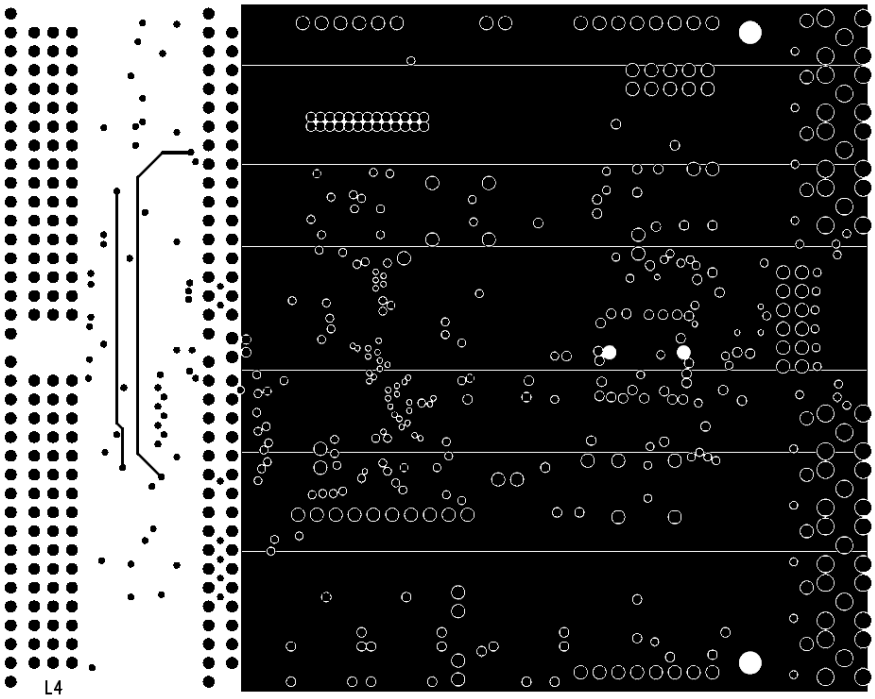
4.2 AM-GPX Board Layout

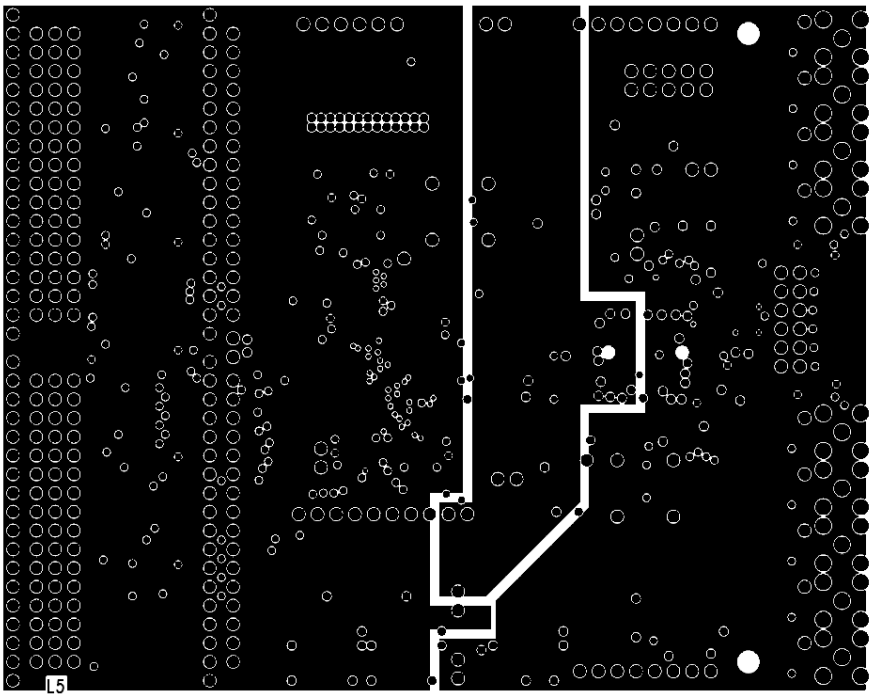


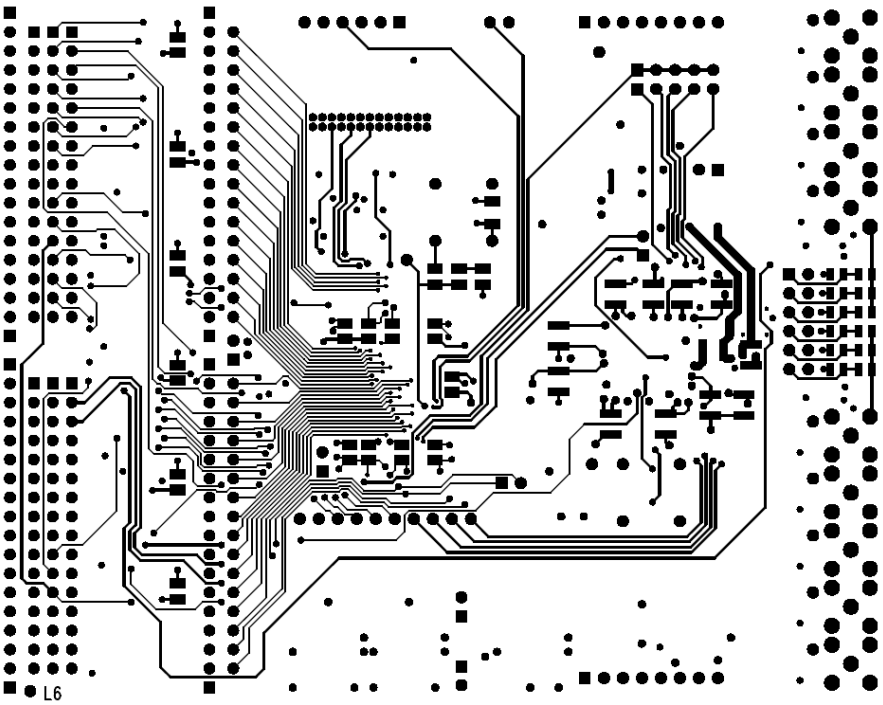


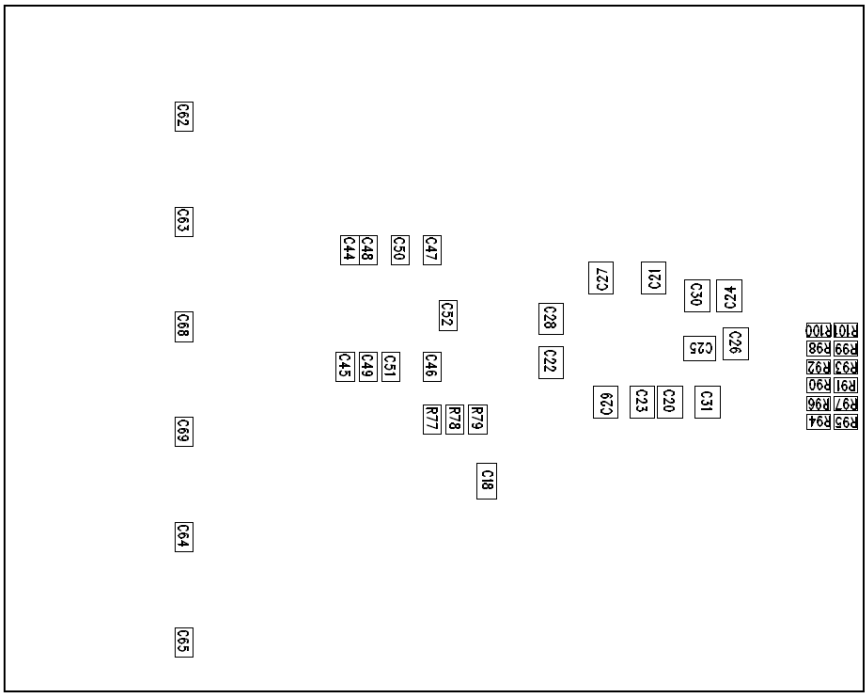

L2


L3


L4


L5

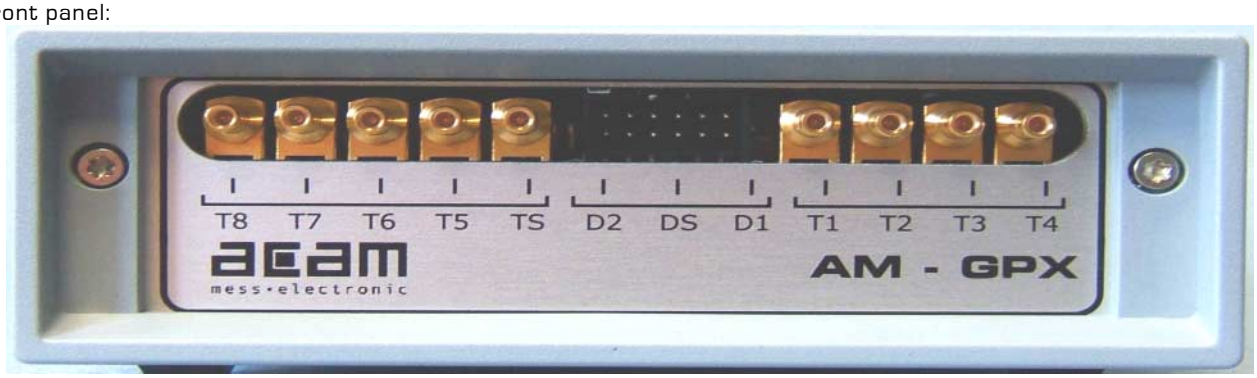

L6


C62
C63
C68
C69
C64
C65
C44
C48
C50
C47
C52
C45
C49
C51
C46
R77
R78
R79
C18
C27
IC2
C30
C24
C28
C22
C25
C26
C29
C23
C20
C31
R101
R100
R99
R98
R93
R92
R91
R90
R97
R96
R95
R94

4.2 Input section

The ATMD-GPX offers 9 Low-voltage TTL inputs and 3 differential Low-voltage PECL inputs.

Front panel:



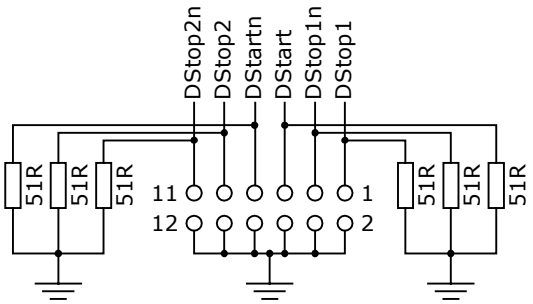
The order of the pins is according to the pinout of the TDC-GPX. This avoids wire crossing on the PCB and the related disturbances.

The connectors are:

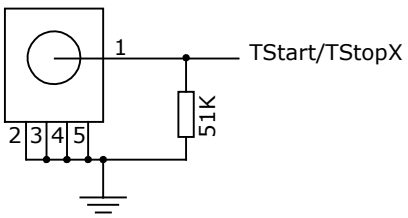
	Jack:
LV-TTL:	SMB
LV-PECL:	Molex

Input circuits:

LV-PECL inputs



LV-TTL inputs



Last Changes:

First edition: 28.7.2004
01.Sep.2004: Section 4
16 Mar 2005: Update to final TDC-GPX version
18 May 2005: Update version 4.0

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