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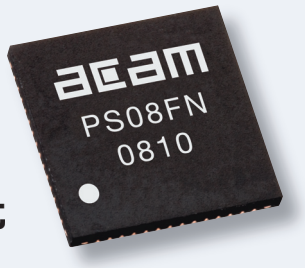
Application Note

Metrological Investigations of PSØ8

Determining Zero Drift and Gain Drift



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Preface

In Juli 2008 acam made zero drift and gain drift investigations with PSØ8 to investigate these important parameters. The capability of PSØ8 to compensate the zero drift and the gain error of the load cell were not content of the tests.

The goals of this investigation were:

- to show the zero- and gain errors of a PSØ8 based electronic
- to get results for mass production values and their stability over several boards
- to investigate if the zero- and gain errors of PSØ8 electronic are small enough to build scales up to 6,000 div. OIML without the need to calibrate each scale (assuming a good load cell is used)

The measurements were made with the evaluation kit using the high end plug-in module. This paper describes how the measurement was done, shows the results and concludes some evidence for those who also want to do these tests.

Making the Tests

The evaluation-kit was connected via the PicoProg programmer to the computer. The PSØ8 evaluation software (version 1.9) was used. All tests were done with 3.6 V supply voltage.

To get the best gain drift behavior, the proper gain correction factor (Mult_PP) has to be set in the PSØ8 register. The optimum value slightly depends on the selected hardware (resistor and capacitor values). With our recommended values for the hardware we have measured the correct gain correction factor (Mult_PP) to 1.32. All measurements were done with this value. If the hardware is changed, the gain correction factor needs to be adapted, which can be done very easily. In the appendix of this application note it is described how to do it.

The tests have been done with 2 different setups.

1. Using the load cell of the PSØ8 evaluation-kit

The first setup used the load cell which comes with the PSØ8 evaluation-kit. Here we took the original equipment of the kit. With every PSØ8 module that we investigated, we took the load cell that was connected to the module.

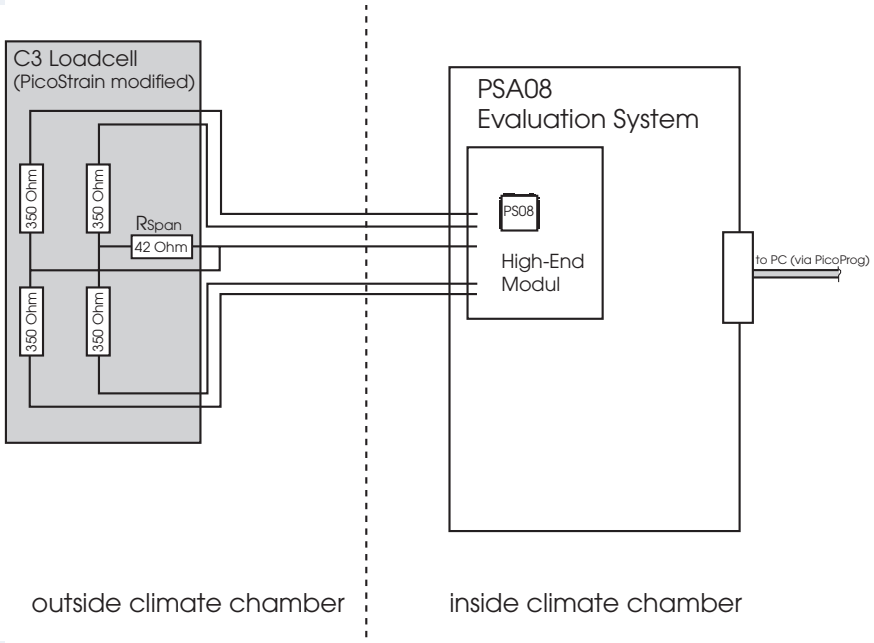

Fig. 1

The load cells were placed outside the temperature chamber and additionally put into a cardboard box to prevent temperature changes during the measurement phase. Only for the short time to put the weight on the load cell, the box was opened.

For the gain drift measurements a 5 kg weight was put on the load cell. The load cells themselves had approximately 1.9 mV/V at 10 kg.

We did not put different weights on the load cell because of the non-linearity of the load cell itself. The used standard C3 load cell has a specified linearity of 0.02% which is 1/5000 or 2gr. related to 10 kg. The linearity of PSØ8 is much higher than that (approx. 0.001%). We proved this with other measurements with a high end load cell and the ALCS350 load cell simulator. Therefore it makes no sense to work with different weights, because we would only show the non-linearity of the different load cells.

1. Using the load cell of the PSØ8 evaluation-kit

The tests were done in the following manner:

- Heat up the electronics in the temperature chamber to +40°C. Start the measurement at this temperature, take the initial offset at +40°C as zero. Put 5 kg on the load cell and take the value.
- Cool with maximum speed to +5°C which takes approx. 15 min. and do the weight measurement with 5 kg again.
- Cooling down to -10°C which takes approx. 15 min. and do the weight measurement with 5 kg again.

During the complete run the software logged all data. After the complete run the offset and gain values can be read from the graph of the software. For the 2 step measurement approx. 3,000 measurement values were logged.

In Fig. 2 such a typical graph can be seen

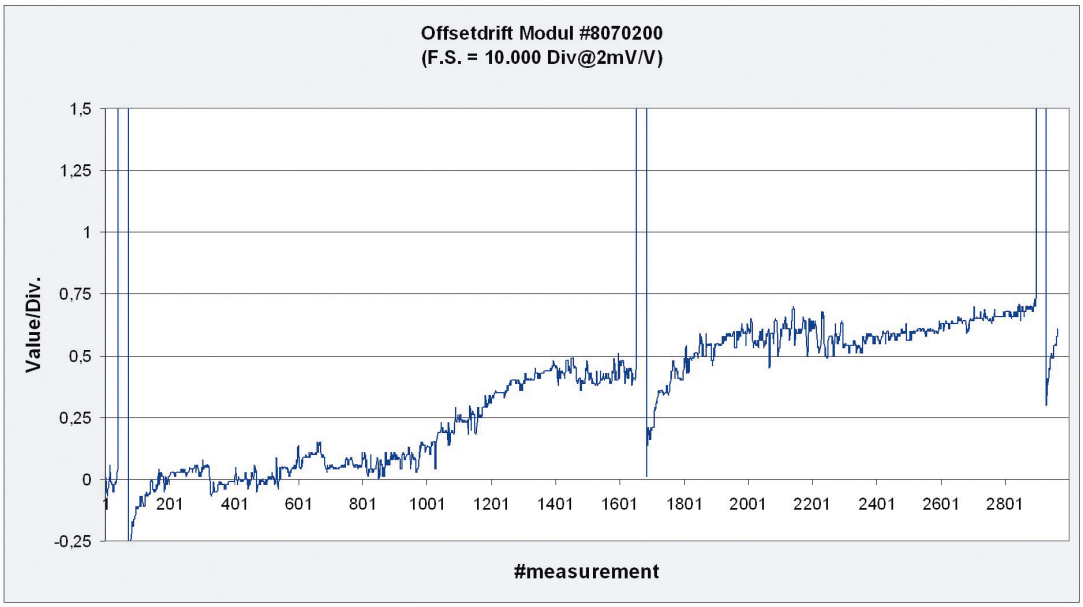

Fig. 2

Fig. 2 shows the graph of a module where the zero drift can be seen.

The values of the different modules were collected in a table. With this test setup 7 modules were measured in total.

1. Using the load cell of the PSØ8 evaluation-kit

Table 1 gives the values:

		Zero Drift nV/K	Gain Drift ppm/K		
No.	# Module	+40°C ...-10°C	+40°C...+5°C	+5°C...-10°C	+40°C...-10°C
1	8070179	24,0	-1,09	0,53	-0,60
2	8070174	38,8	-2,63	-0,57	-2,01
3	8070205	60,2	-2,40	2,30	-0,99
4	8070200	10,3	-1,72	-1,57	-1,67
5	8070207	11,1	-1,99	0,56	-1,22
6	8070197	18,0	-1,05	2,59	0,04
7	8070201	18,7	-1,59	-2,14	-1,75

Table 1

For the zero drift only one value was taken from +40°C to -10°C. For the gain drift the value was split into the value +40°C to +5°C and from +5°C to -10°C and also the summary value +40°C to -10°C was calculated.

Remarks about the measurement

The main problem of these measurements was the influence of the load cell. Two effects make it difficult to investigate the real performance of the PSØ8.

1. Creeping

The load cells showed a creep which is within their specification but nevertheless could not be neglected because we wanted to see the maximum performance of the PSØ8. The creep can be seen very well in Fig. 2. after unloading the load cell . The problem was solved by doing each measurement for exactly 10 sec. and determining the weight from the last value where the load cell was charged to the jump back after unloading it.

2. Sensitivity drift during measurement

It is not easy to protect the (open) load cell against temperature changes during the measurement, even when it is put into a box.

One reason is, that the temperature chamber produces a lot of waste heat when cooling down to -10°C. A second reason is, that after putting the load cell into the cardboard

1. Using the load cell of the PSØ8 evaluation-kit

box the temperature of the load cell changes because the temperature inside the box is different to the former ambient temperature.

Most critical for the load cell is a change of temperature during the measurement. If there is a temperature gradient, a load cell always has additional sensitivity errors. Only in temperature balanced situations a load cell is within specification.

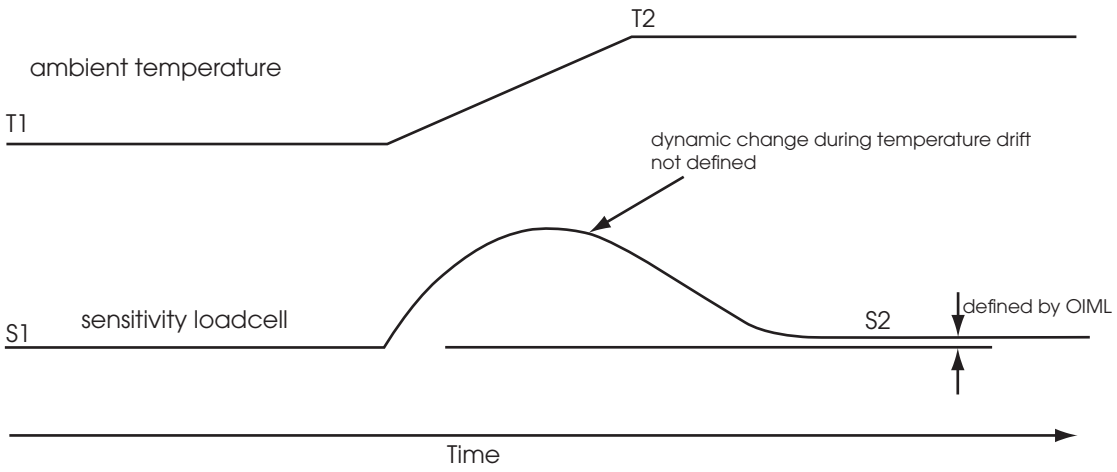

Fig. 3

When temperature changes from T1 to T2, the sensitivity changes from S1 to S2. The difference between the stable levels S1 and S2 are specified by OIML. But when going from T1 to T2 there is a phase where the temperature varies within the load cell. Because of this difference the sensitivity during this time changes a lot. This changing state is not specified and can have a duration in the range of more than one hour. Therefore, when performing OIML measurements, a settling time needs to be waited.

This changes of temperature were the main problem during measurement because it led in some cases to additional errors because the settling time was too short and we had to redo the measurement with a longer settling time. Because of this we did not measure more than 7 modules with the load cell connected in order to save time for making further measurements with a less sensor-sensitive setup.

Nevertheless we showed with the load cell measurements, that all 7 modules are within OIML specification for 6,000 Div at 2mV/V for zero drift and gain drift, even with the described additional errors. You find a more detailed interpretation of the results in the summary of this report.

2. Using a basic load cell simulator

Because of the described problems when using a load cell, we decided to replace the load cell as sensor by a basic load cell simulator after testing 7 modules.

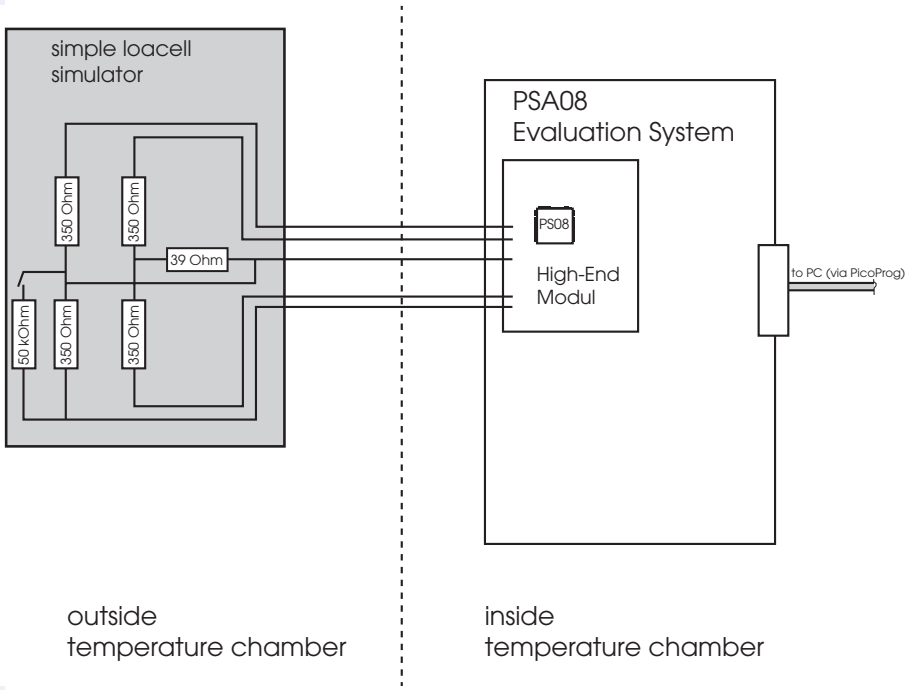

Fig. 4

Fig. 4 shows the new setup. For the 350 Ohm resistors and the 50 kOhm gain resistor, we used high precision resistors with 0.01% accuracy and 0.2 ppm/K temperature drift. For the 39 Ohm Rspan resistor a standard metal film resistor with 2% accuracy and 50 ppm/K temperature drift was used.

We did a reference run with this simple load cell simulator inside the temperature drift chamber where we could verify that the offset drift of the simulator is < 200 nV/K. This is much better than the worst case calculation we did previously based on data sheet values. It can easily be calculated, that the sensitivity drift of the simulator is negligible because of the high stability of the resistors.

With this new test setup we made exactly the same measurements as with the load cells. We measured the gain drift by paralleling a 50 kOhm high precision resistor to one of the bridge resistors, which simulates an excitation of the load cell. The calculated excitation was 1.578076 mV/V or 7,890.38 div. of 10,000 div. at 2 mV/V (taking into account that with TKGain = 0.943 the 39 Ohm Rspan resistor was reduced to 36.43 Ohm. Please see the PSØ8 data sheet for more information about TKGain.)

2. Using a basic load cell simulator

With this setup it was much easier to measure some more modules, because we had not to wait for a long settling time (there is no change in sensitivity) and no creep. In total, 24 modules were measured with this setup. The real performance of the PSØ8 could be investigated.
We got the following results:

		Zero Drift nV/K	Gain Drift ppm/K			
No.*	# Module	+40°C ...-10°C	+40°C...+5°C	+5°C...-10°C	+40°C...-10°C	
8	8070187	5,3	0,80	1,86	1,12	DIS_PP_Cycle_Mod=0
9	8070186	29,0	-0,54	1,86	0,18	
10	8070180	30,0	-0,72	2,37	0,20	
11	8070185	1,5	-0,18	2,62	0,66	
12	8070195	3,7	-0,47	2,71	0,48	
13	8070181	41,0	-1,23	3,21	0,10	
14	8070196	1,2	-0,36	-0,08	-0,28	
15	8070184	5,8	-1,23	3,81	0,28	
16	807018	-6,5	-0,69	1,52	-0,03	
17	8070182	-27,0	-0,54	2,11	0,25	
18	8070194	3,5	-0,98	0,42	-0,56	
19	8070188	16,0	0,15	1,10	0,43	DIS_PP_Cycle_Mod=1
20	8070170	-9,5	0,40	-0,08	0,25	
21	8070175	4,5	0,65	1,52	0,91	
22	8070204	44,0	0,15	-0,85	-0,15	
23	8070173	15,0	0,91	1,02	0,94	
24	8070193	-2,0	0,36	-1,69	-0,25	
25	8070202	9,5	0,76	1,61	1,02	
26	8070208	25,0	0,54	-1,78	-0,15	
27	8070206	6,0	0,66	1,44	0,90	
28	8070172	39,0	-0,29	-0,51	-0,36	
29	8070178	24,0	1,34	0,42	1,07	
30	8070177	1,5	0,80	0,59	0,74	
31	8070172	6,0	-0,29	1,35	0,20	

* we went on with the numbering here from 8 to31to distinguish the first 7 modules with load cell later in the diagrams.

Table 2

During the measurements we recognized, that the PSØ8 internal bit DIS_PP_Cycle_Mod could stabilize the gain drift additionally when set. So we switched on this bit from module 8070188 henceforward.

Discussion of the Results and Conclusion

Defining the limits:

Zero drift:

OIML specifies that the zero drift of the whole scale without zero tracking must not exceed 1 div. within 5°C temperature change. As recommendend in OIML specification we use 50% of this value for the electronics.

The system worked with 3.6 V supply voltage which was also the excitation voltage of the load cell. Therefore the maximum possible zero drift for 2 mV/V can be defined to:

Maximum zero drift for the electronics to reach OIML specification:

3.000 div	→	240 nV/K
6.000 div.	→	120 nV/K
10.000 div.	→	72 nV/K

Gain drift:

OIML specifies that the maximum gain drift of the whole scale must not exceed 1.5 div. over a temperature change of 30°C within the limits -10°C to +40°C. For the electronics we again use 50% of this value.

the summary gain error of the electronics over 30 degrees Celcius must not exceed

3,000 div.	→	250 ppm F.S. (= Full Scale)
6,000 div.	→	125 ppm F.S.
10,000 div.	→	75 ppm F.S.

The maximum gain drift of the electronic can be calculated to

3,000 div.	→	8.3 ppm/K
6,000 div.	→	4.2 ppm/K
10,000 div.	→	2.5 ppm/K

Discussion of the Results

Zero drift

Tables 1 and 2 show that the maximum zero drift is 60 nV/K. The drift behavior over temperature is almost linear. The spread of the offset drift is shown graphically in the diagram below.

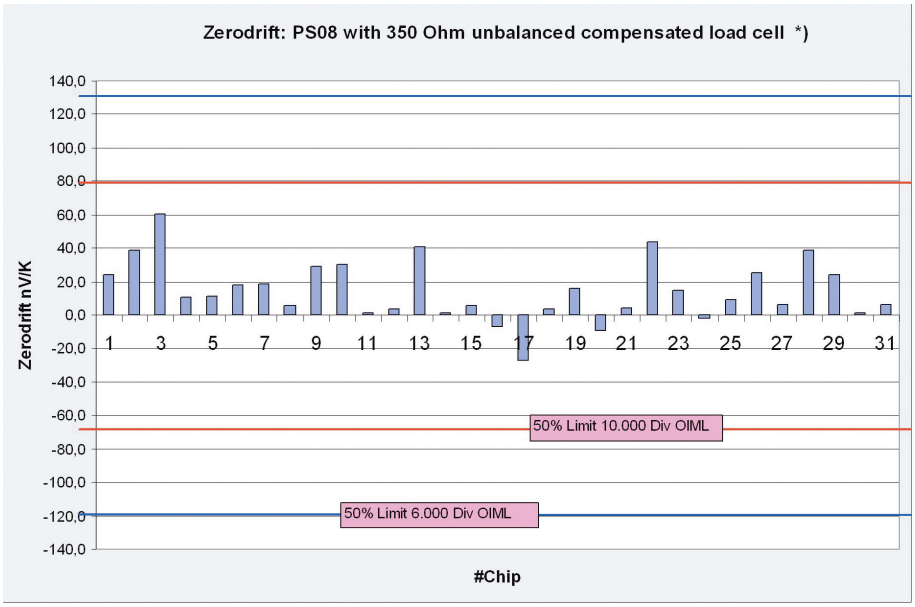

Diagram 1

All measurement results of the zero drift of the 31 modules are within the limit of 10,000 div. For the commonly used 3,000 div. scales there is a very big margin to the limit.

*) unbalanced compensated loadcell means, that only one compensation resistor (Rspan) is used for temperature compensation.

Source of the zero drift

The main source of the remaining zero drift is the PSØ8 itself. Mainly, some wires on the chip that are not matched 100% are responsible for the remaining zero drift. External circuitry like transistors, resistors and capacitors do almost have no effect on the zero drift.

Another important insight is: the higher the strain gage resistor's value, the lower is the zero drift. Because the source of the zero drift are internal uncompensated wire resistors, the drift is lower the higher the strain gage resistors are. The effect has an almost linear

Discussion of the Results

behavior. When using a 1 kOhm strain gage the zero drift is approx. 1/3 of the drift of a 350 Ohm strain gage and will be typically at 5 nV/K.

Gain drift

The gain drift of the modules is not exactly linear. A minimum lies around +5°C. Because of this, we divided the whole temperature range into 2 sections from +40°C to +5°C and from +5°C to -10°C in order to find the true worst case. The first diagram shows the section-splitted summary gain error in ppm of full scale (F.S.) for these 2 temperature ranges and the second diagram shows the summary error over the whole temperature range.

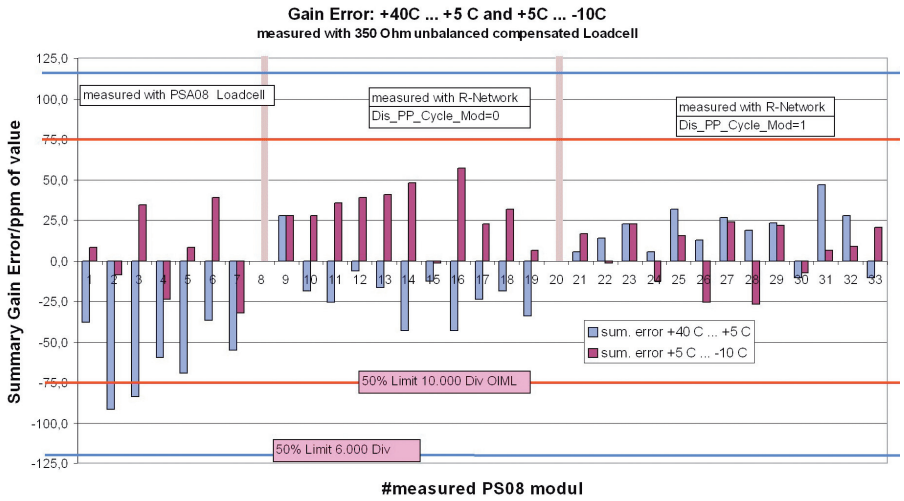

Diagram 2: Summary gain error of splitted temperature ranges

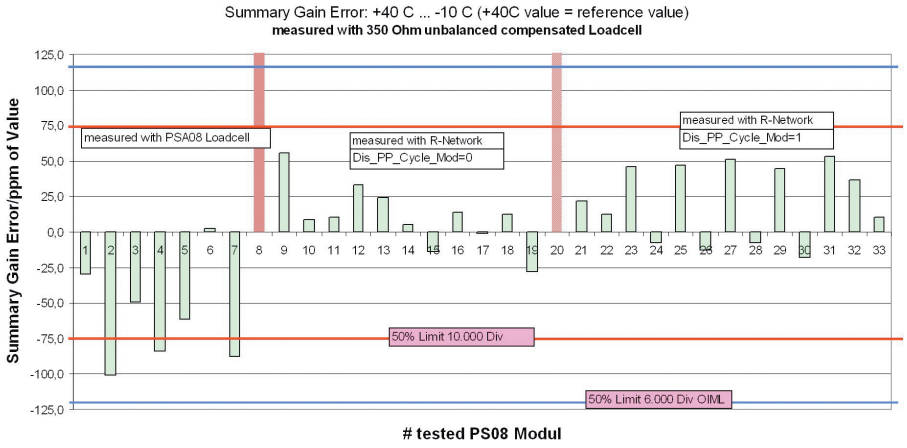

Diagram 3: Summary gain error of full temperature range

Discussion of the Results

The 31 measured modules are divided into 3 domains:

- Measurements with load cell
- Measurements with R-network and bit DIS_PP_Cycle_Mod = 0
- Measurements with R-network and bit DIS_PP_Cycle_Mod = 1

It can be seen very well, that if the internal bit DIS_PP_Cycle_Mod is set, the drift behavior is more stable.

The gain drift of all modules are within the limits of 3,000 div. and 6,000 div. OIML. All the modules measured with the R-network are also within the limit of 10,000 div OIML. For the commonly used 3,000 div. scales there is a very big margin to the limit.

Because of the discussed problems with the temperature behavior of the load cell it is most likely, that also the modules which were measured with the load cell are within the limit of 10,000 div.

Source of the gain drift

The source of the gain drift is the external circuitry of the PSØ8, while the PSØ8 itself has nearly no gain drift om its own. For optimizing the gain drift, the PSØ8 has a gain correction factor (in documentation often called Mult_PP factor). This gain correction factor approximates the nonlinear part of the comparator delaytime with a 2nd order approximation.
In other words, if a very low gain drift is required, this gain correction factor should be applied. In order to do so there are two necessary actions: select the components of the external circuitry properly and secondly, set the proper value for Mult_PP. Once this is done, these settings can be used for the complete production without the need to change this with another production lot of the PSØ8. For the recommended circuitry / hardware we propose corresponding factors for Mult_PP.

Select the components of the external circuitry properly means concrete:

Load capacitor: for a very low gain drift we recommend COG types (e.g. CRM31 series from Murata). Further, with a slight worse gain drift behavior, other types can be used such as the CFCap series from Tayo Yuden. The standard X7R capacitors are not suited for a low gain drift behavior and should only be used in consumer scales.

Discussion of the Results

Blocking capacitor for VCC_LOAD: if a good gain drift behavior also in the negative temperature range is required, the blocking capacitor itself should have a good behavior with negative temperatures also. Most lowest cost **aluminium elcos (electrolytic capacitors) are not suited** and lead to a higher gain drift at negative temperatures. We recommend tantalum electrolytic capacitors for best results also in the negative temperature range. For a 350 Ohm load cell the capacitor's value should be not less than 330 µF. For a 1 kOhm load cell 150-220 µF are sufficient.

Conclusion:
For 3,000 div. and 6,000 div. legal for trade scales it is not necessary to adjust the electronics in any way. The gain- and zero drift is small enough to use predefined values. Especially for cost sensitive 3,000 div. scales PSØ8 gives a very high margin to the limits defined by OIML which allows therefore a cost effective electronic production without the risk to fail in parameters.

Remark:

More than 6,000 div. can be realized with PSØ8 electronic as well, but requires calibration of each scale because of the drift of the load cell. In high end applications with 6,000 div. OIML or more this is done nowadays anyway. Because it is quite hard to find load cells with only a gain drift of 3-4 ppm / K, we recommend the software adjustion of the gain- and offset drift of the whole scale which is offered by the PSØ8. Please contact acam for more information about the possibilites to correct the temperature drift of the whole scale.

Brief summary of the measures for a low gain- and offset drift

We want to summarize all the measures to get a good gain- and offset drift behavior according to the insights of this document. Usually, these measures are given automatically when the design recommendations for PSØ8 are followed.

- Set the internal bit DIS_PP_Cycle_Mod to 1 (register 11, bit 14)
- Use COG or CFCap types as load capacitor
- Use a 330 µF or higher tantal elco as blocking capacitor for VCC_LOAD
- Use the appropiate gain correction factor (Mult_PP) according to your hardware
- Choose the cycle time properly, e.g. 180 µs for a 350 Ohm load cell with 400 nF Cload

Appendix

a. The full data set of the gain measurements

We provide the raw data for those who want to calculate the gain drift by themselves. Full scale for all values is 10,000 div. at 2 mV/V.

The values are only gain values, the zero offset values were subtracted.

No.*	# Module	Value +40°C	Value +5°C	Value -10°C	Type	
1	8070179	4999,35	4999,16	4999,20	Load cell	DIS_PP_Cycle_Mod=**0**
2	8070174	4668,24	4667,81	4667,77	Load cell	
3	8070207	4641,50	4641,11	4641,27	Load cell	
4	8070197	4660,34	4660,06	4659,95	Load cell	
5	8070205	4747,31	4746,98	4747,02	Load cell	
6	8070200	4639,37	4639,20	4639,38	Load cell	
7	8070201	4677,86	4677,60	4677,45	Load cell	
8	8070187	7883,90	7884,12	7884,34	R-network	
9	8070186	7884,03	7883,88	7884,10	R-network	
10	8070180	7883,85	7883,65	7883,93	R-network	
11	8070185	7883,62	7883,57	7883,88	R-network	
12	8070195	7883,25	7883,12	7883,44	R-network	
13	8070181	7883,84	7883,50	7883,88	R-network	
14	8070196	7884,52	7884,42	7884,41	R-network	
15	8070184	7884,48	7884,14	7884,59	R-network	
16	8070183	7884,72	7884,53	7884,71	R-network	
17	8070182	7885,12	7884,97	7885,22	R-network	
18	8070194	7884,33	7884,06	7884,11	R-network	
19	8070188	7881,22	7881,26	7881,39	R-network	DIS_PP_Cycle_Mod=**1**
20	8070170	7880,84	7880,95	7880,94	R-network	
21	8070175	7881,28	7881,46	7881,64	R-network	
22	8070204	7881,10	7881,14	7881,04	R-network	
23	8070173	7880,89	7881,14	7881,26	R-network	
24	8070193	7881,40	7881,50	7881,30	R-network	
25	8070202	7881,37	7881,58	7881,77	R-network	
26	8070208	7881,12	7881,27	7881,06	R-network	
27	8070206	7880,67	7880,85	7881,02	R-network	
28	8070172	7881,37	7881,29	7881,23	R-network	
29	8070178	7880,86	7881,23	7881,28	R-network	
30	8070177	7880,88	7881,10	7881,17	R-network	
31	8070192	7880,68	7880,60	7880,76	R-network	

Table 3

Appendix

b. Determining the gain correction factor (Mult_PP)

As mentioned earlier, the gain drift of the PSØ8 can be adjusted very close to zero by selecting the proper Mult_PP factor. If a well-chosen Mult_PP factor exists and the hardware is not changed, the value can be used over the complete production (even if there are different production lots of the PSØ8 used).

With the recommended hardware we determined following Mult_PP factors:

a. For electronics which uses **external** comparator with our recommended values: 1.32
b. For electronics which uses **internal** comparator with our recommended values: 1.19

Case a. is applied on the high end module of the PS08 evaluation-kit and case b. is used on the standard module of the kit.

Besides these approved values for Mult_PP we want to explain the determination of the proper Mult_PP factor shortly in case you want to determine it by yourself or in case the hardware is changed.

Dependencies of the gain correction factor (Mult_PP)

Low-pass capacitor

The gain drift of the PSØ8 electronics comes mainly from the delaytime of the comparator. This delaytime depends on the value of the low pass capacitor which is parallel to the collector resistor of the comparator transistor. We recommend 4.7 kOhm for the collector resistor and 3.3 nF for the parallel capacitor. If this capacitor is changed, the optimum Mult_PP factor changes too. This is the main dependency of Mult_PP from the hardware, besides the general selection between external and internal comparator.

Example:
A reduction from 3.3 nF to 1.0 nF will reduce the optimal Mult_PP factor from 1.32 to 1.23.

There is no reason to change the optimal value of 3.3 nF for the parallel capacitor, but in case it is done, please be aware of the effects on Mult_PP.

Appendix

There are further dependencies of Mult_PP with only a small influence:

- Load capacitor (we recommend 400 nF for a 350 Ohm load cell)
- Blocking capacitor of VCC_LOAD (we recommend 330 uF or 680 uF), do not choose less than 330 uF, please use tantalum electrolytic capacitors.
- Supply voltage (if it is possible in the application, we recommend 3.6V)
- Cycle Time (we recommend 180 us with 400 nF load capacitor and 350 Ohm load cell)

These parameters will affect the optimum Mult_PP factor only slightly. If one ore more changes have been made in the schematic of a new product, it may be necessary to determine the proper Mult_PP factor again.

The behavior between the Mult_PP factor and the resulting gain drift is very linear: a new Mult_PP factor can be determined easily, as the following section shows.

Determining new Mult_PP factor in case of hardware changes

Make 2 measurements with 2 different Mult_PP factors in the temperature chamber. Have a look at the gain drift in both runs and than calculate the new optimal Mult_PP by simple linear mathematics.

Example:

Run1:
Mult_PP=1.2 [MPP1] shows a gain drift of –4 ppm/K [GD1]
(with higher temperature the gain decreases)

Run2:
Mult_PP=1.4 [MPP2] shows a gain drift of +6 ppm/K [GD2]
(with higher temperature the gain increases)

A change of Mult_PP by 0.2 results in a change of the gain drift by 10 ppm/K or in other words, a change of 0.01 of Mult_PP results in a gain drift change of 0.5 ppm/K. Applied on the gain drift of –4 ppm/K at Mult_PP factor = 1.2 it means to increase the factor by 0.08. Calculation: (4ppm / 0.5ppm) x 0.01 = 0.08. That means, in this case the new optimum Mult_PP factor [MPPN] is 1.2 + 0.08 = 1.28.

Appendix

Run3:
Verifiy the gain drift with the new Mult_PP factor of 1.28.

The formula for calculating the proper Mult_PP factor is:

$$MPPN = MPP1 - \frac{GD1 \times (MPP2 - MPP1)}{GD2 - GD1}$$

The newly determined Mult_PP factor [MPPN] remains unchanged for the whole production, if the same hardware values are used.