TDC-GPX – Reduced Decoupling

This note is a supplement to application note no. 13, "TDC-GPX – PLL Regulation Circuit"

The intention is to show possibilities to reduce the number and size of the decoupling capacitors in the TDC-GPX supply circuit. We propose the following capacitors for the different power supply blocks:

1.	Vddo	Data bus I/O supply	TQFP pins 17, 40, 54 FBGA pins G3, L6, L12	100 nF per pin
2.	Vddo	I/O supply	TQFP pins 2,98,94,91,86,82,81,77 FBGA pins B1,A3,C4,C5,B7,A9,B9,A11	Connect all pins to a common copper plane and place two 100nF capacitors close to pins 77/A11 and 98/A3
3.	Vddc	Core supply	TQFP pins 1, 10, 39, 69, 79 FBGA pins A1, F1, M7, E12, B10	Connect a capacitor to each side of the chip TQFP pins 10, 39, 69, 79 FBGA pins F1, M7, E12, B10
			Standard: 4 x 47 µF Derating (increase of standard deviation) with smaller capacities: 4 x 10 µF up to 200ns: no effect up to 500ns: about 4ps up to 1000ns: about 15ps 4 x 22 µF up to 200ns: no effect up to 500ns: about 2 ps up to 1000ns: about 7 ps	
4.	Vddc-o Vddc-h	Hardmacro supply	TQFP pins 87, 88 FBGA pins C6, A7	One capacitor to each pin and the voltage regulator output
			Standard: 1 x 100 µF at regulator out and 2 x 47 µF at the pins The regulator decoupling can be reduced to 10 µF without a negative effect Derating (increase of standard deviation) with smaller capacities at the pins: 2 x 10 µF up to 200ns: no effect up to 500ns: about 4 ps up to 1000ns: about 10 ps 2 x 22 µF up to 200ns: no effect up to 500ns: about 2 ps up to 1000ns: about 5 ps